Sheet 1 of 1

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO. 501.43228X00	SERIAL NO.
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT MURATA, et al.	
		FILING DATE January 14, 2004	GROUP

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
✓	AA	5,198,683	03/30/1993	SIVAN	357	67	05/03/1991
✓	AB	5,670,803	09/23/1997	BEILSTEIN, Jr. et al.	257	278	02/08/1995
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	AE						
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Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract Yes	Abstract No
✓	AM	11-176936	07/02/1999	JP	H01L	21/768	X	
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✓	AU	WATANABE, et al., "A Novel Circuit Technology with Surrounding Gate Transistors (SGT's) for Ultra High Density DRAM's", IEEE Journal of Solid-State Circuits, Vol. 30, No. 9, September 1995
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Examiner	Date Considered
	07/05/05